formed over the thin layer of silicon 140 and an intervening gate insulator layer 142, is used together with the source/drain regions to create a SOI transistor.

**In the Claims:**

Please add the following new claims:

24. *(New)* A method for analyzing a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of circuitry in the die; and

directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing and, therefrom, analyzing the die.

25. *(New)* The method of claim 24, wherein inducing a detectable response therefrom as a function of the portion of the circuitry failing includes detecting a change in secondary electrons emitted from the exposed region of the insulator.

26. *(New)* The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an uninhibited emission of secondary electrons.

27. *(New)* The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an inhibited emission of secondary electrons.

28. *(New)* A method for detecting logic states of a plurality of circuit nodes in a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed and adjacent to the plurality of circuit nodes;

inputting electrical signals to the die to cause the plurality of circuit nodes to take on logical states; and

scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes adjacent to the exposed region upon which the electron beam is directed and, therefrom, detecting the logic states of the plurality of circuit nodes.

29. *(New)* The method of claim 28, wherein scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes comprises:

detecting a non-positive logical state at one of the plurality of circuit nodes as a function of detecting an uninhibited emission of secondary electrons; and

detecting a positive logical state at one of the plurality of circuit nodes as a function of an inhibited emission of secondary electrons.

## Remarks

Favorable reconsideration of this application is requested in view of the following remarks. For the reasons set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The Office Action mailed on January 29, 2003, indicated that the traversals of the Section 112(2) rejections are not accepted; that the Section 112(2) rejections of claims 1 and 16 have been removed; claims 1, 16 and 20 stand rejected under §112(2) as being incomplete; claims 1, 2, 8-11, 16-21 and 23 stand rejected under §§102(a) and 102(e) as